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Effects of DC-link Filter on Harmonic and Interharmonic Generation in Three-phase Adjustable Speed Drive Systems

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***Abstract*—Harmonic and interharmonic distortions are considered as the main power quality issues especially in the distribution networks. The double-stage Adjustable Speed Drives (ASDs) in which the front-end diode rectifier is connected to a rear-end inverter through an intermediate DC-link filter may inject significant amount of harmonics and interharmonics into the grid and consequently degrade the grid power quality. In this paper, the effect of the DC-link filter – as a key player – on the ASD input current harmonic and interharmonic distortions is investigated. In this respect, the ASD performance is evaluated harmonically based on three different DC-link configurations; the conventional filter (with AC- and/or DC-side chokes, and DC-link capacitor), the Small DC-Link Capacitor (SDLC), and the controlled DC link by using an Electronic Inductor (EI) technique. It shows how employing the small DC-link capacitor will push the harmonics into the higher frequency ranges and it will also give rise to more interharmonic distortions. Moreover, the EI configuration is introduced as an optimal DC-link intermediate circuit within the investigated frequency range of 0–2 kHz. The presented analysis and discussions have been validated by the simulation and experimental results.**

Index Terms—Adjustable speed drives, DC-link filter, harmonics, interharmonics, voltage source converter.

I. Introduction

The growing integration of power electronics devices into the grid, and consequently the harmonic and interharmonic injections has raised concerns about the power quality degradation in the future electrical networks. Meanwhile, the ASDs with the capability of energy saving and also flexibility in control, have attracted more attentions in several industrial and residential applications [1]. Whereas, the harmonic and interharmonic distortions generated by the ASDs would make them as one of the main contributors to the grid harmonical pollutions [2]–[6]. In this respect, various investigations have been initiated to decrease the side effects of employing the ASDs by using the passive and active harmonic compensation techniques [7]–[9].

In the conventional ASD system, which is still the most common structure in the industrial applications, a large electrolytic capacitor is used in the DC link to store energy and to power the rear-end inverter with a rather low DC-link voltage variation, as it is shown in Fig. 1(a). In this condition, a large AC- and/or DC-side choke is also required in order to smooth the input current distortions. Consequently, a simple and reliable approach can be achieved at the cost of being bulky and expensive and also with a limited lifetime for the electrolytic capacitor.

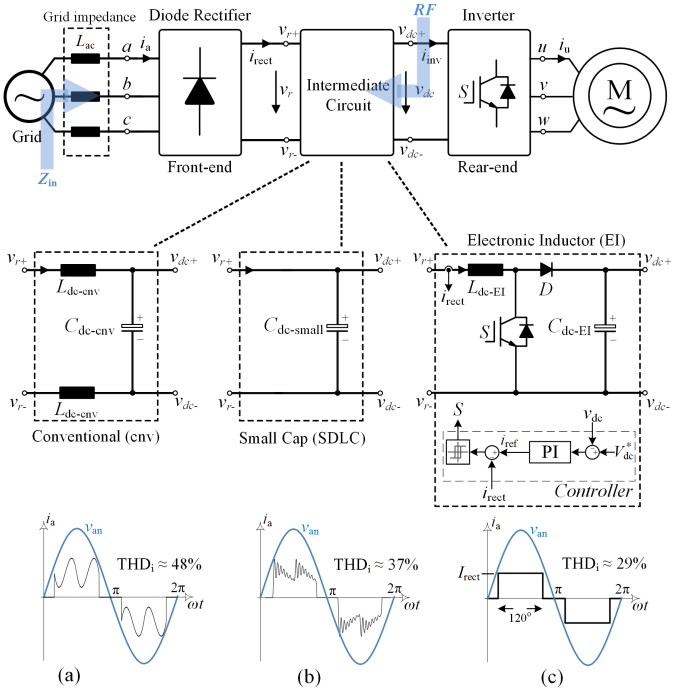

Fig. 1. Typical block representation and corresponding input current waveform of the double-stage Adjustable Speed Drive (ASD), (a) with conventional DC-link filter, (b) with small DC-link capacitor, (c) with Electronic Inductor (EI).

Recently, the ASD system with embedded small DC-link film capacitors, as represented in Fig. 1(b), has gained more attentions [3], [10], [11], where capacitor lifetime span and system power density can be elevated. Since the small film capacitor used in this structure cannot store high levels of

energy, a large voltage variation occurs across the DC-link capacitor. As a result of the natural commutation of the three-phase diode rectifier, more charging and discharging states would occur in this condition and it will give rise to a different input current harmonic distribution compared to the conventional drive. Moreover, the large DC-link voltage variations make it necessary to apply a suitable control strategy on the rear-end inverter.

Besides employing the ASD systems with the passive filter configurations, continuous efforts have been dedicated to use active filtering solutions [12], [13]. Fig. 1(c) shows the EI structure as an intermediate circuit to improve the line current harmonic distortions. In this method, the EI is controlled to behave like an infinite inductor and to provide a constant current at the immediate DC terminal of the three-phase diode rectifier. Consequently, the hump-shape input current waveforms in the conventional drive case will be replaced by a 120°-pulse width square shape current waveforms with applying the EI technique, and better input current harmonic performance can be achieved.

The main goal in this paper is to analyze and discuss about the input current harmonic and interharmonic distortions in the double-stage ASD systems, where three different kinds of the DC-link intermediate circuits have been employed between the front-end three-phase diode rectifier and the inverter; the conventional filter (with a large AC- and/or DC-side chokes and a large DC-link capacitor), the small DC-link capacitor, and the controlled DC-link filter through applying the EI technique. Notably, the investigation has been performed with respect to the frequency range of 0–2 kHz.

II. Harmonic Distortions

In order to analyze the harmonic distribution patterns in the double-stage ASD systems as shown in Fig. 1, it is essential to accurately model the impedance characteristics seen from both sides of the Point of Common Coupling (PCC). In the low voltage distribution networks, the line side impedance is usually determined by the size and type of the step-down transformers. Consequently, the transformer leakage inductances L_{ac} are considered as the dominant factor, which will affect the drives performance. As for the converter

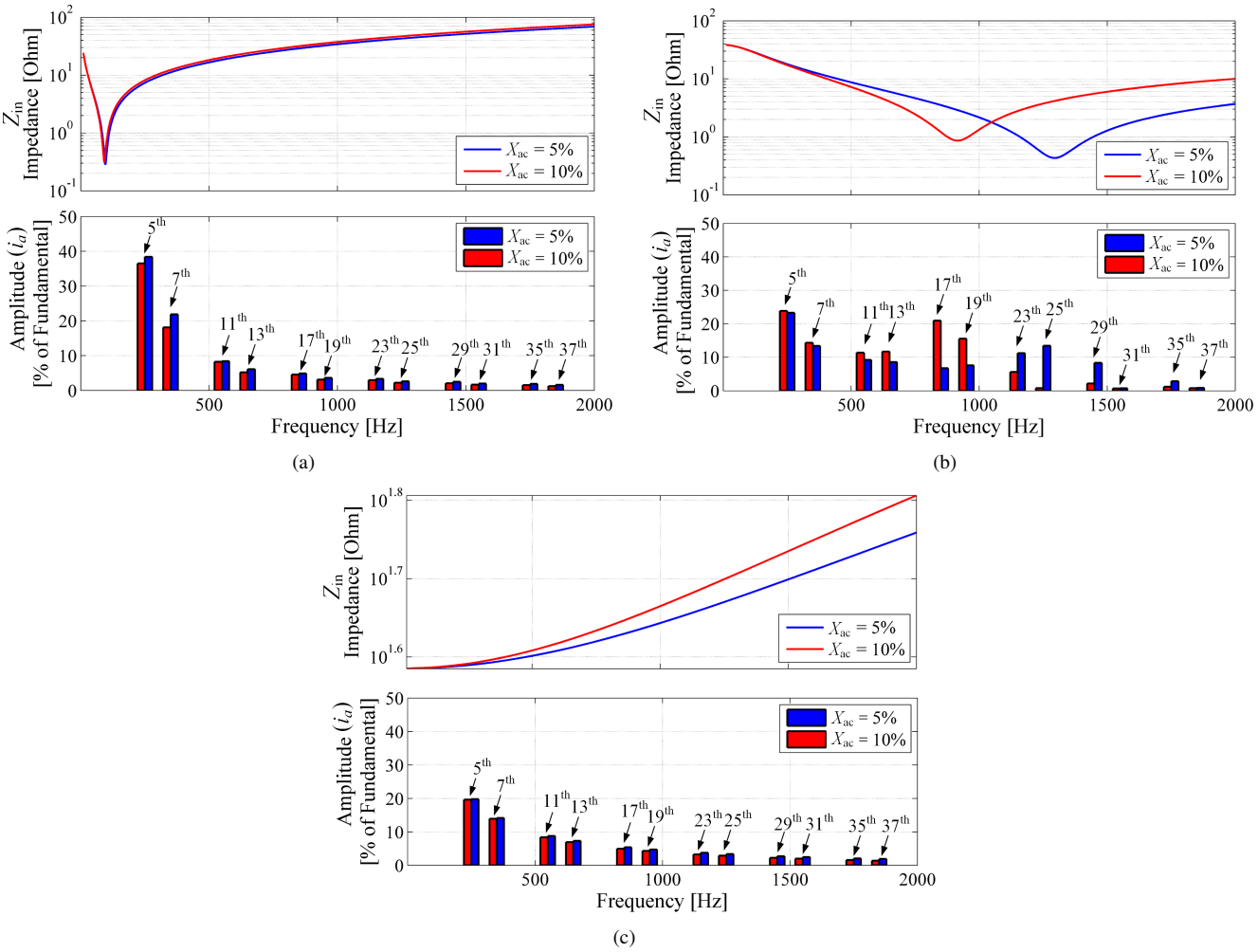

Fig. 2. Simulated impedance characteristic and input current harmonic spectrum of (a) Conventional , (b) SDLC, and (C) Electronic Inductor (EI), ASDs with 5% and 10% AC side reactance values, when the drives work in the full load power (i.e., 7.5 kW).

TABLE I
PARAMETERS OF THE ASDs SYSTEM (FIG. 1).

Symbol	Parameter	Value
$v_{a,b,c}$	Grid phase voltage	230 V_{rms}
f_g	Grid frequency	50 Hz
P_b	Grid base power	100 kVA
L_{dc-cnv}	Conventional DC-link inductor	1.25 mH
L_{dc-EI}	EI's inductor	2 mH
C_{dc-cnv}	Conventional DC-Link capacitor	500 μF
$C_{dc-small}$	SDLC capacitor	30 μF
C_{dc-EI}	EI's capacitor	470 μF
v_{dc-EI}	EI's DC-link voltage	700 V
k_p, k_i	EI's voltage controller parameters	0.05, 1.5
HB	EI's controller hysteresis band	0.88
v_{LL}	Induction motor rated voltage	380 V_{rms}
P_{IM}	Induction motor rated power	7.5 kW

side, the DC-link intermediate circuits and the load power levels are the main factors influencing the ASDs input current harmonic distributions.

The input impedance characteristic of the investigated ASD systems from the grid point of view along with the corresponding drives input current harmonics distribution have been shown in Fig. 2, based on the system parameters listed in Table I. In this study, particular emphasis is also given to the role of the transformer leakage L_{ac} effects on changing the drives harmonics. In this respect, the drives performance have been evaluated at different reactance levels (X_{ac}=5–10% of the system base impedance value). Notably, the detailed impedance-based analysis with respect to the employed drive systems have been addressed in [14].

Fig. 2(a) shows the input impedance characteristics and also the input current harmonics spectrum of the conventional drive with the transformer reactance values of 5 and 10%. It is worth to note that by employing the large DC-link inductor and capacitor in the conventional drive applications, the impedance characteristics usually will see a resonance at low frequencies (i.e., below 150 Hz), and consequently it will not affect higher order harmonics existing in the input current. Moreover, as it can be observed in Fig. 2(a), the large filter components in the conventional drives will significantly reduce their performance sensitivity with respect to the grid side impedance variations. Contrary to the conventional drives with bulky DC-link capacitor, in SDLC ASDs, the resonance frequency at the impedance characteristic will be pushed to higher frequency levels and it may magnify the high-frequency harmonics. This issue has been clearly addressed in Fig. 2(b), where the resonance frequencies are in well agreement with the corresponding amplified input current harmonics. Moreover, using the small DC-link capacitor will significantly affect the drive sensitivity with respect to the grid side impedance values. As it can be seen in Fig. 2(b), the transformer reactance variation from 5% to 10% will give rise to the resonance frequency variation from about 1300 Hz to 900 Hz, respectively.

In order to highlight the better performance of active DC-link filters, impedance characteristics of an EI drive is considered as the third case and the results are presented in Fig. 2(c).

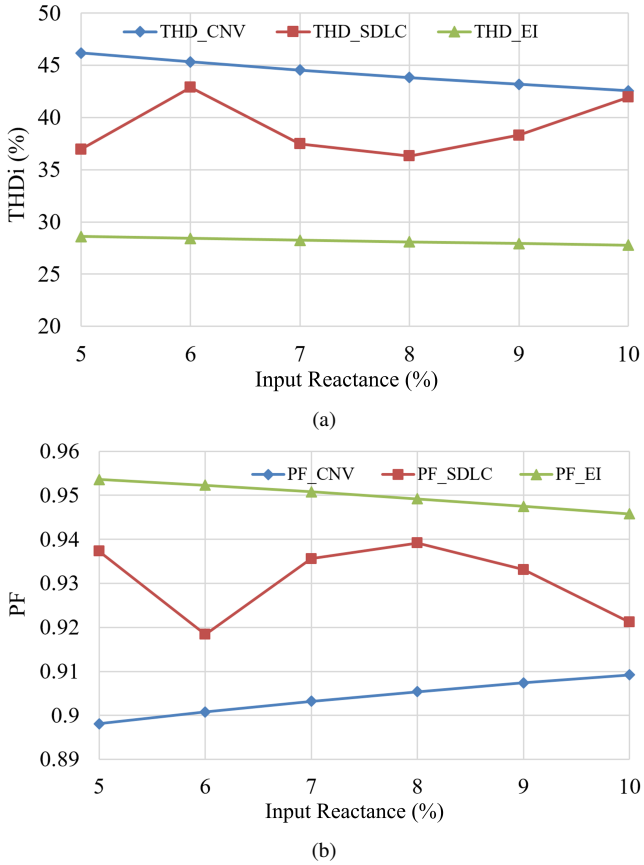

Fig. 3. The ASDs input current, (a) Total Harmonic Distortions (THD$_i$) and (b) Power Factor (PF), with respect to the AC line reactance variations, when the drives operate at full load power (i.e., 7.5 kW).

As it was expected, emulating an infinite DC-link inductor via using the EI technique will lead to a high impedance characteristic and without imposing a resonance frequency within the investigated frequency range. Consequently, the input current harmonics will reduce unanimously as the frequency increases.

The input currents Total Harmonic Current Distortion (THD$_i$) and Power Factor (PF) in the employed ASD systems have been shown in Fig. 3 with respect to the transformer reactance variations. Notably, the presented results are associated with the rated operating conditions of the ASDs (i.e., 7.5 kW). Based on Fig. 3, the EI drive improves the THD$_i$ and PF compared to the other two ASD systems. Although, the SDLC drive shows better harmonic performance compared to the conventional drives at the rated power, but their dependency on the grid impedance may give rise to stability issues [15].

From the system level perspective, it is important to consider the ASDs harmonic performance in respect to the grid stiffness. The grid stiffness can be measured through the short circuit ratio $R_{sce} = S_{sc}/S_n$, with S_{sc} and S_n stating the grid short circuit and the drive nominal apparent power, respectively. Actually, having a general picture – both the amplitude and the phase information – of the harmonic emissions of the ASDs at different short circuit levels will help to determine the maximum harmonic levels of the three-phase and the single-

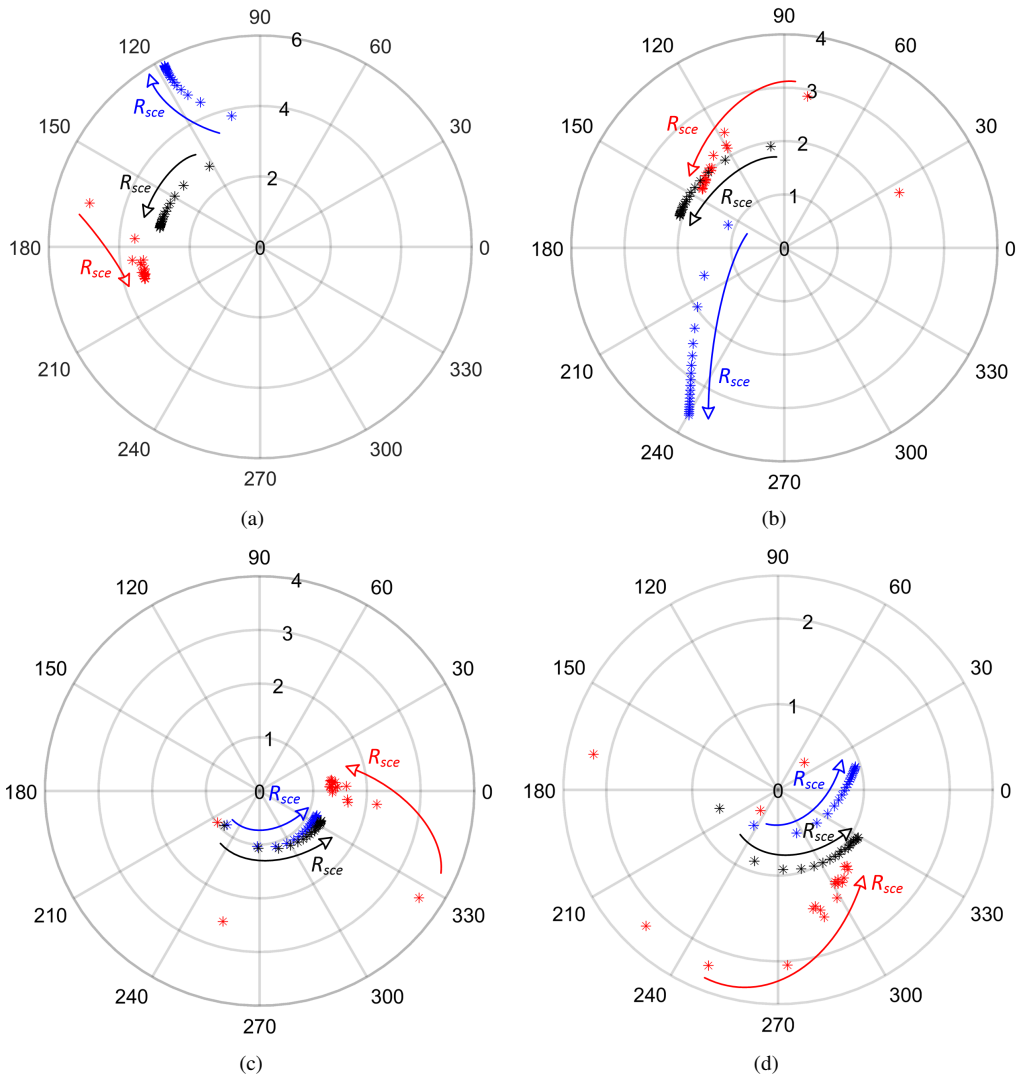

Fig. 4. Polar plot of the ASDs input current i_a harmonics as a function of R_{sce}=20–400 with a step of 20. *:Conventional drive, *:Small DC-link drive, *:EI drive. (a) 5th harmonic current, (b) 7th harmonic current, (c) 11th harmonic current, and (d) 13th harmonic current.

phase ASDs in the power system.

In order to assess this issue in the ASD systems to be considered, the harmonical behaviour of the drives has been evaluated at several short circuit ratios R_{sce}=20–400 with a step of 20. In this analysis, the ASDs are connected to the grid via a transformer with the secondary side line-to-line voltage v_{ab} = 400 V and a per unit impedance value of Z_{ac} = R_{ac} + jX_{ac}= 1% + j5%. Fig. 4 shows the polar plots of the main current harmonic components (i.e., the 5th, 7th, 11th, and 13th harmonics) of the employed ASDs with respect to the grid short circuit variations. As it can be observed, the dispersed distribution of the harmonics in the SDLC drive, especially at lower short circuit ratios, and at higher frequency harmonic components, demonstrates that the SDLC drives harmonic characteristic is highly dependent on the grid short circuit level R_{sce}, whereas a more anticipated behaviour can be observed in the conventional and EI drive cases. This makes the harmonic characteristics of the SDLC drives unpredictable, especially when multitude of these drives are connected to the Point of Common Coupling (PCC).

III. Interharmonic Distortions

This section investigates the performance of the employed ASDs from interharmonics perspective. In the double-stage ASD systems shown in Fig. 1, the rear-end inverter usually feeds the motor load via applying a specific Pulse Width Modulation (PWM) strategy at the demanded frequency and power levels. Notably, the Space Vector Modulation (SVM) and the Discontinuous Pulse Width Modulation–30° lag (DPWM2) are the most popular modulation methods in the ASD applications. As a result of the applied modulation technique, the pulsating voltage waveforms v_x (x = u, v and w) will be generated at the inverter pole terminals (see (1)), where they are composed of a DC offset, baseband harmonics (of the fundamental output frequency f_o), harmonics of the carrier frequency f_c, and carrier sidebands located around the carrier components [16]:

$$v_x(t) = \frac{A_{00}}{2} + \sum_{n=1}^{\infty} [A_{0n}\cos(n[\omega_o t - p\frac{2\pi}{3}]) + B_{0n}\sin(n[\omega_o t - p\frac{2\pi}{3}])] + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} [A_{mn}\cos(m\omega_c t + n[\omega_o t - p\frac{2\pi}{3}]) + B_{mn}\sin(m\omega_c t + n[\omega_o t - p\frac{2\pi}{3}])] \quad (1)$$

with m and n representing the carrier group and baseband group index, respectively. A_{0n}, B_{0n}, A_{mn}, and B_{mn} denote the harmonic coefficients, which should be obtained according to the associated modulation methods applied on the inverter. The fundamental and carrier angular frequencies are stated as ω_o and ω_c. The parameter p will choose 0, 1 and -1 for the output phases u, v, and w. Based on balanced load condition, the frequency domain output currents $I_x(\omega)$ (x = u, v and w) are calculated utilizing the load phase impedance $Z(\omega)$ in the frequency domain as,

$$\begin{bmatrix} I_u(\omega) \\ I_v(\omega) \\ I_w(\omega) \end{bmatrix} = \frac{V_{dc}}{3Z(\omega)} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} S_u(\omega) \\ S_v(\omega) \\ S_w(\omega) \end{bmatrix} \quad (2)$$

It is worth to note that the well-known inverter switching functions $S_x(\omega)$ (x = u, v and w) are usually represented as s_x = v_x/V_{dc}, with V_{dc} being the DC value of the DC-link voltage. By assuming that the inverter operates as a loss less system, the contribution of the output side currents i_x (x = u, v and w) to the DC-link inverter side current i_{inv} can be obtained as,

$$i_{inv}(t) = S_u(t) \cdot i_u(t) + S_v(t) \cdot i_v(t) + S_w(t) \cdot i_w(t) \quad (3)$$

At the DC-link stage, the inverter side oscillations i_{inv} coming from the load side will be significantly influenced by the DC-link transfer function, which is called as the Resonance Factor (RF) and it is given as,

$$RF = \left| \frac{i_{rect}}{i_{inv}} \right| \quad (4)$$

Fig. 5 represents the resonance factors corresponding to the drive systems to be considered. It can be observed that in the conventional drive system, the inverter side current harmonics will remain almost constant at the frequency range $f <\sim 60$ Hz, they will be magnified at ~ 60 Hz$< f <\sim 200$ Hz with a resonance peak around 150 Hz, and also will be attenuated at $f >\sim 200$ Hz, when they pass through the DC link. Whereas in the SDLC ASD system, the resonance peak will occur at high frequency (around 2500 Hz) and the DC link would not act as a very low pass filter against the output side oscillations. Consequently, the DC-link rectifier side current i_{rect} will inherit much more harmonics (of the output fundamental frequency) compared to the conventional drive case. This issue will be worse if the inverter operates at low switching frequency, which it is the case in many ASD applications. As for the DC-link resonance factor associated with the EI drive, it can be seen in Fig. 5 that it imposes a

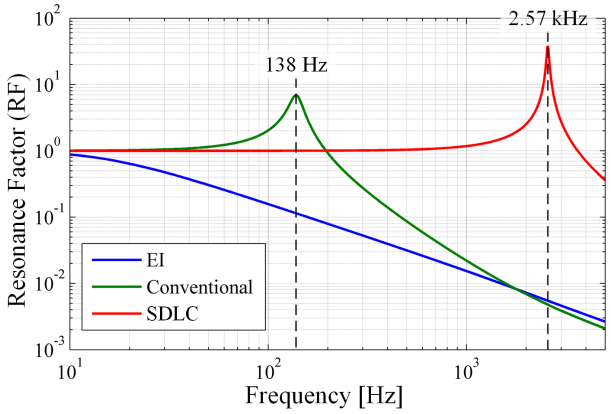

Fig. 5. Equivalent DC-link Resonance Factors (RF), corresponding to the Conventional, Small Capacitor and EI drives.

significant attenuation on the inverter side current harmonics, which can give rise to lower amplitude harmonics distortion at the DC-link rectifier side compared to the other two ASD configurations. Finally, the DC-link rectifier side oscillations, which have already been caused by the inverter operation and have passed through the DC stage, will be modulated by the front-end diode rectifier switching function as $S_{ph}(t)$,

$$i_{ph}(t) = S_{ph}(t)\mathrm{i}_{rect}(t) \quad (5)$$

Since the ASDs normally supply the motor loads at the frequencies other than the grid fundamental frequency, the multiplication of the DC-link rectifier side harmonics (of the output frequency) with the front-end diode rectifier switching functions generates the interharmonic components in the grid side currents. Meanwhile, the higher amplitude DC-link rectifier side current harmonics will result in the higher amplitude line current interharmonic distortions.

Interharmonic distortions can be evaluated through different analysis principles. In this work, the grouping approach suggested by the IEC standard has been used for interharmonics assessment. Based on IEC 61000-4-7 standard [17], a Discrete Fourier Transform (DFT) performed over a Rectangular time Window (RW) of exactly ten cycles for 50 Hz system or exactly twelve cycles for 60 Hz systems, corresponding to a time window width (T_w) of 200 ms is recommended for harmonic and interharmonic grouping measurement. In this respect Interharmonic Subgroup (ISG) of amplitude $C^2_{n+0.5-200-ms}$ is defined as,

$$C^2_{n+0.5-200-ms} = \sum_{k=2}^{8} C^2_{10n+k} \quad (6)$$

where C_i represents the rms value of the DFT output. As for the grouping results presented in this paper, in order to provide further smoothed values, an average over 15 contiguous time windows (3-s intervals) is applied [17].

Fig. 6 shows the measured input current interharmonic subgroup values in the conventional, SDLC and EI drives, when the motor operates at the output frequency f_o=36 Hz and the power P=4 kW. Notably, the interharmonic subgroups order

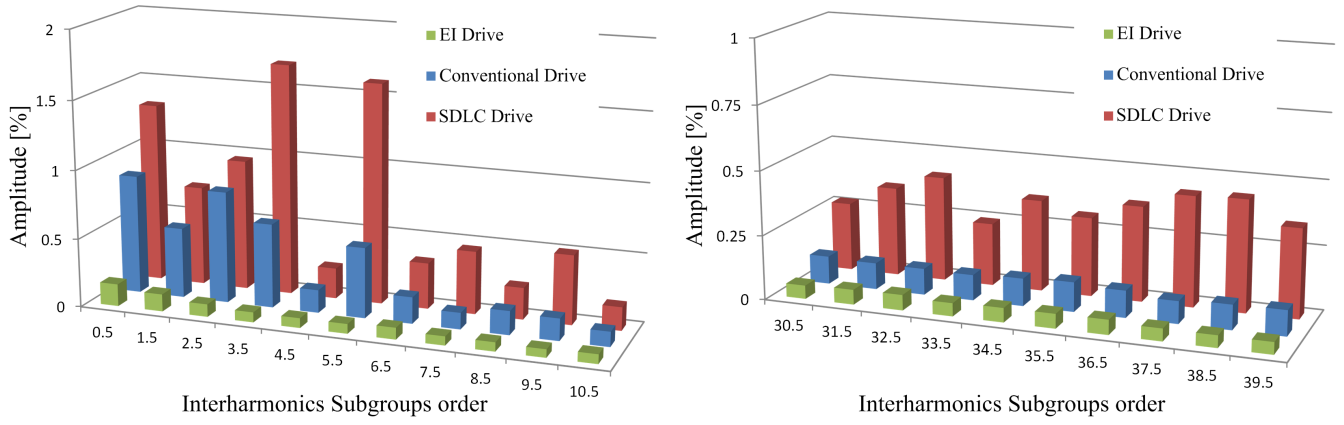

Fig. 6. Measured input current interharmonic subgroup values of the conventional, SDLC and EI ASDs, (a) within the frequency range 0–500 Hz, (b) within the frequency range 1500–2000 Hz, when the ASDs operate at the output frequency f_o = 36 Hz, the load power P = 4 kW and by using the symmetrical regularly sampled SVM modulation technique on the inverter.

0.5, 1.5, 2.5, ..., 10.5 are corresponding to the frequency ranges [10–40], [60–90], [110–140], ..., [510–540] Hz, respectively. Moreover, the interharmonic subgroups order 30.5, 31.5, 32.5, ..., 39.5 are related to the frequency ranges [1510–1540], [1560–1590], [1610–1640], ..., [1960–1990] Hz, respectively.

As it can be seen from Fig. 6(a), the SDLC drive generates higher amplitude interharmonic subgroup values in the low frequency range of 0–500 Hz, compared to the other two ASD systems. Besides, the lowest interharmonic subgroup values are associated with the EI drive. As for higher order interharmonic subgroups illustrated in Fig. 6(b), it is clear that the SDLC drive will inject much more interharmonics into the line currents with respect to the conventional and EI drives. This issue is in well agreement with the discussion presented for the effects of the DC-link intermediate circuit on the output side harmonic transfer.

IV. Conclusion

In this paper, the input current harmonic and interharmonic distortions of the double-stage ASD systems have been evaluated by considering three different types of the DC-link intermediate circuit (the conventional filter with the large AC- and/or DC-link inductors and capacitor, the small DC-link capacitor and the electronic inductor). The grid side harmonic currents on each case have been addressed by performing the impedance-based analysis. It has been shown that the harmonic performance of the ASD systems with the small DC-link capacitor depends significantly on the line side reactance values. However, it may inject lower total harmonic current distortions into the grid, especially in the full load conditions compared to the conventional drives. Moreover, it is demonstrated that the SDLC drives may inject much higher interharmonics into the grid due to introducing a weak filtering at the DC-link stage against the harmonic currents coming from the load side. The ASD systems with the electronic inductor-based intermediate circuit have shown better harmonic and interharmonic performance in respect to other two ASD systems.

Although the presented analysis highlight the better performance of applying the active filtering technique (i.e., by using the EI drive), in order to gain a better insight on performance of each technique the effect of loading profile should be considered. This is due to the fact that motor drive applications commonly operate under partial loading condition which can significantly deteriorate input current quality and damping of the DC-link filter. Therefore, the future work will be focused on investigating loading profile condition in addition to the considered grid stiffness. Moreover in this paper, the effects of the DC-link filter on the drives interharmonic emissions have been analyzed by using the symmetrical regularly sampled SVM modulation technique. However, it would also be of great interest to evaluate the effects of other modulation strategies (e.g., random frequency, random pulse position and etc.) on the drive input current interharmonics, when different DC-link technologies are employed.

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